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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/606,530 | 06/26/2003 | Eric Mendenhall | N9186 | 5744 |

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| EXAMINER | |
|---|---|
| WILLOUGHBY, TERRENCE RONIQUE | |
| ART UNIT | PAPER NUMBER |
| 2836 | |

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/606,530 | MENDENHALL, ERIC |
| | Examiner | Art Unit |
| | Terrence R. Willoughby | 2836 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on 26 June 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/29/03, 10/20/03, 5/10/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 15-20 are rejected under 35 U.S.C. 102(b) as being unpatentable by Stanley (US 4,330,809).

With respect to claim 15, Stanley teaches the claimed said protection method, comprising the steps of: generating a power estimate of power dissipated by a power transistor (Column 2, lines 14-19); filtering the power estimate to eliminate any transient power estimates and to generate a filtered power estimate (Fig. 2, 38); and comparing the filtered power estimate to a predetermined power limit and, when the filtered power estimate exceeds the predetermined power limit, generating a power transistor control signal (Fig.1, 20) that causes the power transistor to reduce its power dissipation (Column 1, lines 19-34).

With respect to claim 16, Stanley teaches the claimed said steps of adjusting the filtered power estimate so that it varies as a function of power transistor operating temperature (Column 2, lines 27-33).

With respect to claim 17, Stanley teaches the claimed said steps of limiting current output by the power transistor to a predetermined maximum level (Column 3, lines 14-31)

With respect to claim 18, Stanley teaches the claimed said power transistor control signal (Fig. 1, 20 and Column 1, lines 26-29) causes the power transistor (Fig. 1,10) to reduce its power dissipation by reducing power supply voltage (Column 3, lines 16-18) applied to the power transistor.

With respect to claim 19, Stanley teaches the claimed said power transistor control signal (Fig. 1, 20 and Column 1, lines 26-29) causes the power transistor (Fig. 1,10) to reduce its power dissipation by reducing base current (Column 3, lines 14-16) flowing into the power transistor.

With respect to claim 20, Stanley teaches the claimed said power transistor control signal (Fig. 1, 20 and Column 1, lines 26-29) causes the power transistor (Fig. 1, 10) to reduce its power dissipation by reducing power supply voltage applied to the power transistor and reducing base current flowing into the power transistor (Column 3, lines 14-31).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-11,13. are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art and in view of Stanely (US 4,330,809).

With respect to claim 1, the acknowledged prior art as shown in Figure 5 teaches the claimed said protection circuit comprising: a transistor power estimation circuit (Fig.

5, R1, R2, R3 and Re); a transistor control circuit (Fig. 5, Q1 and D1); a transistor maximum current limiting circuit (Qout) connected to the power estimating circuit. The acknowledged prior art lacks the claimed said power estimate filtering circuit and the transistor temperature adjustment circuit, both connected to the power estimating circuit. However, Stanley teaches the claimed power estimating filtering circuit (Fig. 1 14) connected to the operational amplifier (Fig. 1,16) and temperature comparator (Fig. 1,18). It would have been obvious to those skilled in the art at the time the invention was made to provide the filtering network circuit and temperature comparator of Stanley in the power estimating circuit taught by the acknowledged prior art and also connecting the filtering network circuit to the transistor control circuit to determine the instanteous applied power to the transistor by determining the simulated differential in temperature between the die of the transistor and its heat sink. A control circuit monitors the sensed die temperature during transistor operation and when a predetermined maximum is reached, the applied power to the transistor is reduced to prevent the transistor from excessive overheating and damage.

With respect to claim 2, the acknowledged prior art as shown in Figure 5 R1, R2, R3 and Re teaches the claimed said transistor power estimation circuit includes: a transistor current sensing circuit (Fig. 5, Re); a voltage sensing circuit (Fig. 5, R2); a summing circuit (Fig. 5, R1, R2, Re) connected to the transistor current and voltage sensing circuits.

With respect to claim 3, the acknowledged prior art as shown in Figure 5

teaches the claimed said transistor power estimation circuit is single slope power estimation.

With respect to claim 4, the acknowledged prior art as shown in Figure 6 teaches the claimed said transistor power estimation circuit is a two-slope power estimation circuit as mentioned in the specification of the applicant, page 22, lines 1-2.

With respect to claim 5, the acknowledged prior art as shown in Figure 6 and Figure 8 teaches the claimed said transistor power estimation circuit is a two-slope power estimation circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a resistor and diode network connected between the voltage network divider to cause a change in the protection threshold slope. The resistor and diode addition to the circuit will cause a breakpoint in the voltage output of the transistor and the threshold slope and will allow the power transistor to more reliably operate in safe operating area (SOA). This would provide a four-slope power estimation circuit.

With respect to claim 6, the acknowledged prior art as shown in Figure 6 and in Figure 8 teaches the claimed said transistor power estimation circuit is a two-slope power estimation circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add two or any number of additional resistor diode networks as needed which are connected between the voltage network divider to cause a change in the protection threshold slop. The resistor and diode addition to the circuit will cause four additional breakpoints in the voltage output of the transistor. This

continuous procedure will allow the power transistor to operate in more accurate region than the four-slope power estimation circuit.

With respect to claim 7, Stanley teaches the claimed said power estimate filtering circuit includes an averaging circuit (Fig. 2, 38) and (Column 3, lines 10-13)

With respect to claim 8, Stanley teaches the claimed said power estimate filtering circuit (Fig. 2, 38) includes a transistor thermal equivalent circuit (Column 2, lines 64-68).

With respect to claim 9, Stanley teaches the claimed said power estimate filtering circuit (Fig. 2, 38) includes a resister (Fig.2, 40) capacitor (Fig. 2, 42) network.

With respect to claim 10, the acknowledged prior art as shown in Figure 5 teaches the claimed said maximum current limiting circuit (R1, R2, R3, and Re) includes a predetermined number of diodes ( D1) and a resistor (Re, R1, R2, R3).

With respect to claim 11, the acknowledged prior art as shown in Figure 5 teaches the claimed said transistor control circuit (Q1 and D1) includes a transistor (Q1).

With respect to claim 13, Stanley teaches the said transistor temperature adjustment circuit integrated into the power transistor (Column 3, lines 14-16).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over acknowledged prior art in view of Stanely (US 4,330,809) and further review of Bodge (3,781,839).

With respect to claim 12, Stanley teaches the claimed said temperature adjustment circuit (Fig. 1, 18 and Fig. 2, 48). Stanley lacks the claimed said thermistor.

However, Bode teaches the claimed said thermistor (Abstract, lines 4-8). It would have been obvious to those skilled in the art at the time the invention was made to include a thermistor taught by Bodge to sense the temperature amount through the power transistor using a resistor, because the use of temperature information from a thermistor increases the accuracy of the thermal protection arrangement.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over acknowledged prior art in view of Stanely (US 4,330,809) and Knudsen (US 5,734,261).

With respect to claim 14, Knudsen teaches the claimed said control circuit includes an optocoupler (Abstract, lines 1-7). It would have been obvious to those skilled in the art at the time the invention was made to include an optocoupler taught by Knudsen in the control circuit acknowledged prior art as mentioned in claim 1 to providing a current and voltage limited protection to the power transistor when triggered by the control circuit.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bishop (US 3,979,745) and in view of Wyland (US 6,039,471).

With respect to claim 21, Bishop teaches the claimed steps for using a piecewise linear approximation (Column 1, lines 33-36); varying the piecewise linear approximation as a function of transistor temperature (Column 1, lines 14-20); averaging the temperature varying (Column 1, lines 25-28). Bishop does not specifically mention that this method is applied to estimate junction temperature of a transistor. However, Wyland teaches that it is known to estimate junction temperature of a electronic components (Abstract, lines 1-4 and 17-20). It would have been obvious to

one of ordinary skill in the art at the time the invention was made to use the piecewise linear approximation curve method taught by Bishop to generate a estimate of the power dissipated in a transistor taught by Wyland to accurately track the power dissipation using the piece linear approximation method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRW

Phuong T. Vu
Patent Examiner